AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) An operational amplifier circuit, comprising:

a first inverted amplifier circuit that receives a first input signal;

a second inverted amplifier circuit that receives a second input signal;

a third inverted amplifier circuit that receives an estimated common-mode output signal and an output signal of said first inverted amplifier circuit and outputs a first output signal and a second output signal;

a fourth inverted amplifier circuit that receives the estimated common-mode output signal and an output signal of said second inverted amplifier circuit and outputs a third output signal and a fourth output signal;

a first non-inverted amplifier circuit that receives the estimated common-mode output signal and outputs an output signal, the output signal of the first non-inverted amplifier circuit fed back to the output signal of the first inverted amplifier circuit; and

a second non-inverted amplifier circuit that receives the estimated common-mode output signal and outputs an output signal, the output signal of the second non-inverted amplifier circuit fed back to the output signal of the second inverted amplifier circuit,

wherein adding the second output signal and the fourth output signal generates the estimated common-mode output signal.

2. (Original) The operational amplifier circuit according to claim 1, wherein the first and second input signals are differential input signals.

3. (Original) The operational amplifier circuit according to claim 1, further comprising:

a fifth inverted amplifier circuit that receives an output signal of the first inverted amplifier circuit and outputs an output signal that is fed back to the output of the first inverted amplifier circuit;

a sixth inverted amplifier circuit that receives an output signal of the second inverted amplifier circuit and outputs an output signal that is fed back to the output of the second inverted amplifier circuit;

a seventh inverted amplifier circuit that receives an output signal of the first inverted amplifier circuit and outputs an output signal that is fed back to the output of the second inverted amplifier circuit; and

an eighth inverted amplifier circuit that receives an output signal of the second inverted amplifier circuit and outputs an output signal that is fed back to the output of the first inverted amplifier circuit.

4-11. (Canceled)

12. (Currently amended) A sample/hold circuit comprised of an operational amplifier circuit according to claim 1 and a capacitor that is selectively connected to the operational amplifier circuit.

13. (Original) A filter circuit comprised of a first stage integrator using the operational amplifier circuit according to claim 1 and subsequent stage integrators.

14. (Canceled)